AMENDMENTS TO THE CLAIMS

Claim 1 (original): A method for scheduling tasks in a wafer processing system comprising:

defining a plurality of operations that can be run on said wafer processing system;

adding at least one of said plurality of operations to an operation list;

switching an operation in said operation list to an active state; and

scheduling all operations in said operation list that are in the active state to run on said wafer processing system.

Claim 2 (original): The method of claim 1 wherein each of said plurality of operations includes conditions for adding an operation to said operation list.

Claim 3 (original): The method of claim 1 wherein each of said plurality of operations includes conditions for switching an operation in the operation list to an active state.

Claim 4 (original): The method of claim 1 wherein said plurality of operations includes a recipe operation.

Claim 5 (original): The method of claim 1 wherein said plurality of operations includes a recipe operation and a non-recipe operation.

Claim 6 (currently amended): A wafer processing system including a computer, said computer having a computer readable storage memory containing a plurality of operations that can be run on said wafer processing system, said computer readable storage memory further containing instructions for (a) adding at least one of said plurality of operations to an operation list, (b) switching an operation in said operation list to an active state, and (c) scheduling all operations in said operation list that are in the active state to run, wherein at least one operation in the operation list including a sequence of actions for performing fabrication steps on a semiconductor wafer.

Claim 7 (original): The wafer processing system of claim 6 wherein each of said plurality of operations includes conditions for adding an operation to said operation list.

Claim 8 (original): The wafer processing system of claim 6 wherein each of said plurality of operations includes conditions for switching an operation in the operation list to an active state.

Claim 9 (original): The wafer processing system of claim 6 wherein at least one of said plurality of operations is a recipe operation.

Claim 10 (currently amended): A data structure for an operation to be performed on a wafer processing system comprising:

a first level including conditions for adding said operation to an operation list and conditions for switching said operation to an active state, said operation list including at least one operation for performing fabrication steps on a semiconductor wafer; and

a second level including a sequence of actions to be performed on said wafer processing system.

A1 Cont'd

Claim 11 (currently amended): The data structure of claim 10 wherein said first level further includes a list of modules to be used by said operation, at least one module in the list of modules including a wafer processing chamber.

Claim 12 (original): The data structure of claim 10 wherein said operation is a recipe operation.

Claim 13 (original): The data structure of claim 12 wherein said second level further includes a list of wafers to be processed in accordance with said recipe operation.